REMARKS

In view of the above amendments and the following remarks, reconsideration is requested.

The Title of the Invention was objected to as not being clearly indicative of the invention to which the claims are directed. Accordingly, the Title of the Invention has been amended to "Tracking Error Detection Apparatus Including Reduction in False Tracking Error Detection During Phase Error Detection."

Minor editorial amendments have been made to the specification and abstract. It is submitted that no new matter has been added to the application via such amendments. A substitute abstract along with a marked-up copy of the substitute abstract are filed herewith.

A replacement Fig. 6 is filed herewith to amend the "valid edge" beneath the difference $\Delta 1$ to correctly indicate that the binary signal B falls before the binary signal A as is evident from the zero cross points of phase comparison inputs A and B which result in the difference $\Delta 1$.

Claim 4 was rejected under 35 U.S.C. § 112, second paragraph as being indefinite. This rejection is traversed.

Claim 4 has been amended to more explicitly recite the operations of the phase difference detection circuit.

Fig. 4 shows an example of a tracking error detection apparatus which includes a phase difference detection unit 22. The phase difference detection unit 22 performs the operations of invalid edge cancellation, phase difference calculation, pulse generation, and data updation via its constituent components, i.e., the invalid edge cancel unit 5, the phase difference calculation unit 1, the pulse generation unit 2, and the data updation unit 6, respectively. Please note that the phase difference calculation unit 1 is a component of the phase difference detection unit 22.

Claim 4 is definite in that it recites operations of the phase difference detection unit, i.e., performing phase comparison, judging whether the edges are valid or invalid, and selectively performing output/updation. Claim 5 more specifically recites the constituent components of the phase difference detection unit and their operations.

It is submitted that a person having ordinary skill in the art would understand from the disclosure that the operations of the phase difference detection unit are the operations of its constituent components. Accordingly, claim 4, which recites the operations of phase difference detection unit is definite and complies with 35 U.S.C. § 112, second paragraph.

Claims 1-3, and 8-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the acknowledged prior art in view of Kanno. This rejection is traversed and is inapplicable to claims 1, 2, 8, and 9 as amended. Claims 3 and 10 have been canceled.

Claim 1 has been amended to include limitations similar to those previously found in claim 3, and claim 8 has been amended to include limitations similar to those previously found in claim 10.

Thus, claims 1 and 8 recite phase difference detection circuits that limit a result of phase comparison to a value under a first predetermined value when the result of phase comparison is larger than the first predetermined value, that the first predetermined value is a maximum value of the tracking error signal, and that the maximum value is based on a relationship between a shortest pit length and a track pitch of the optical disc to be played.

For example, please consider Figs. 3(a) and 3(b) which illustrate the optical disc to be played having a shortest pit length of 0.27 μm, (which is 3T, where 1T is equal to one channel clock of the recording/playback system), and a track pitch of 0.74 μm. In such a case, the maximum value the tracking error signal can legitimately attain is 2T. Since the phase difference is directly calculated from a distance between zero-cross points, a value obtained as a result of the phase comparison should not exceed the maximum value of the tracking error signal, which is 2T in this case. Thus, in this example, the "first predetermined value" is set as 2T, which is the maximum value of the tracking error signal based on a relationship between a shortest pit length and a track pitch of the optical disc to be played.

Rather than limiting a result of phase comparison to a value based on a relationship between a shortest pit length and a track pitch of the optical disc to be played as recited in claims 1 and 8, Konno discloses a method of judging the type of disc (CD or

DVD) based on the pit density (column 10). In Konno, in order to judge a type of optical disc (especially CD v. DVD) on the basis of differences between pulse widths of phase error signals, pulse width limitation is performed so that a pulse having a pulse width equal to or larger than the predetermined pulse width does not appear in pulse trains of the phase error signal. The pulse width limit value is set in such a manner that the pulse width limitation operation has no affect on the phase error signal of a DVD due to its high pit density but does affect the phase error signal for a CD due to its low pit density. Accordingly, if a tracking error signal is generated based on the phase error signal after pulse width limitation is performed, tracking error signals which are generated are greatly different in amplitude for a CD verses a DVD, and thereby it can be judged whether the disc is a CD or DVD.

Thus, the pulse width limit in Konno is set to a value whereby the limit will affect CD's only and not DVD's. The setting of the pulse width limit of Konno is not based on the a relationship between a shortest pit length and a track pitch of the optical disc to be played as recited in claims 1 and 8.

In view of the above, no obvious combination of the teachings of Konno with the acknowledged prior art would result in the apparatuses recited in claims 1, 2, 8, or 9. Therefore, it is submitted that claims 1, 2, 8, and 9 are allowable over the prior art of record.

Claims 4 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over acknowledged prior art in view of Konno and Nakajima. This rejection is traversed.

Claim 4 recites an edge detection circuit for detecting the states of edges of binary signals of sampling data of two digital signals, and that each of the two digital signals is obtained by adding output signals from the two photoreceptor elements positioned on a diagonal line. Claim 11 recites a first edge detection circuit for detecting the states of edges of binary signals of sampling data of two digital signals respectively obtained from the two photoreceptor elements positioned forward in the advancing direction of the information track, among the four digital signals, and a second edge detection circuit for detecting the states of edges of binary signals of sampling data of two digital signals respectively obtained from the two photoreceptor elements positioned backward in the advancing direction of the information track, among the four digital signals.

Contrary to the edge detection circuits discussed above and recited in claims 4 and 11, the edge detection circuit 11 of Nakajima detects falling edges of a binary signal indicating a result of comparison between a total sum of signals outputted from four areas of the photodetector 2 and a reference voltage +Ref 4. In other words, the edge detection circuit 11 of Nakajima detects the falling edges of the binary signal indicating the magnitude of the quantity of reflected light (column 7, lines 31-43), but does not detect the states of edges of binary signals such as recited in claims 4 and 11, i.e., signals which are subjected to phase comparison.

In view of the above, no obvious combination of the teachings of Nakajima, Konno and the acknowledged prior art would result in the apparatuses recited in claims 4 or 11. Therefore, it is submitted that claims 4 and 11 are allowable over the prior art of record.

Claims 5-7 and 12-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art in view of Konno and Nakajima, and further in view of Hayashi. This rejection is traversed.

First, please refer to the discussion above regarding the edge detection circuits recited in claims 4 and 11, which detect edges in two signals from various combinations of photodetector elements. Claims 5 and 12 each recite invalid edge cancel units for judging whether edges detected by edge detection circuits are "valid" or "invalid," and data updation units for maintaining the output level of the output data until the next phase comparison end pulse occurs, when the result of judgment by the invalid edge cancel unit is "valid," while maintaining the output level of the data that has been outputted at the just-previous phase comparison end pulse, when the result of judgment in the invalid edge cancel unit is "invalid."

Hayashi does not disclose or suggest such features. Rather, Hayashi discloses an invalid pulse elimination circuit 125 for removing an invalid edge pulse from an edge detection signal "wbpe" that is obtained by detecting the edges of the corrected wobble signal. This invalid pulse elimination circuit removes an invalid edge pulse by using a window "wbwin" that is generated by a window generation unit 126. As shown in Figs. 31 and 33, the invalid pulse elimination circuit 125 receives the edge detection signal "wbpe" and the window "wbwin," and removes the edge pulse of the edge detection

signal "wbpe" outside High-level intervals where the window "wbwin" is open (column 34, lines 15-44). Thus, the invalid pulse elimination circuit 125 merely removes the invalid edge detection pulses from the edge detection signal "wbpe" using the window, but does not judge whether the edges to be targets of phase comparison, (i.e., the signals from combinations of photodetector elements), are "valid" or "invalid" based on the state of these edges. Thus, Hayashi also fails to disclose or suggest maintaining an output level until a next phase comparison end pulse occurs, when edges are judged as "valid," or maintaining the output level from the just-previous phase comparison end pulse, when the edges are judges as "invalid." Moreover, Hayashi therefore also fails to disclose or suggest the specific comparisons of states of edges of two signals as recited in claims 6, 7, 13, and 14.

In view of the above, no obvious combination of the teachings of Hayashi, Nakajima, Konno and the acknowledged prior art would result in the apparatuses recited in any of claims 5-7, and 12-14. Therefore, it is submitted that claims 5-7, and 12-14 are allowable over the prior art of record.

Accordingly, it is submitted that claims 1, 2, 4-9, and 11-14 are allowable over the prior art of record and that the present application is in condition for allowance. The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

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ABSTRACT OF THE DISCLOSURE

A tracking error detection apparatus comprises a photodetector comprising plural photoreceptor elements; zerocross detection circuits for detecting zerocross points at which two sequences of digital signals intersect the center levels of the respective digital signals, which digital signals are generated according to the amounts of light received by the respective photoreceptor elements and are outputted from the photodetector; a phase difference detection circuit for performing phase comparison using a distance between zerocross points of the two sequences of digital signals, and outputting a result of phase comparison; and a low-pass filter for performing band restriction to a signal outputted from the phase difference detection circuit~~, thereby to obtain a tracking error detection apparatus~~. When a phase difference between the two sequences of digital signals, which is detected by the phase difference detection circuit, is larger than a maximum value of a theoretical tracking error signal, the output from the phase difference detection circuit is limited.